WHAT IS CLAIMED IS:

1. A wavelet transformation circuit comprising:

a set of data inputs;

a bank of shift registers, for loading a succession of pixel value from a digital image, each successive pixel value being loaded at a preselected clock interval;

a set of coefficient registers that correspond to said bank of shift registers, for storing coefficient values implementing a wavelet filter;

a multiplier/accumulator circuit that generates, at said preselected clock interval, a result based on application of said coefficient values against the succession of pixel values stored by said bank of shift registers; and

at least one result register for storing said result.

2. The circuit of claim 1, wherein said wavelet transformation engine operates under control of a digital signal processor (DSP).

3. The circuit of claim 2, wherein said DSP controls a memory for storing a digital image as a sequence of pixel values.

4. The circuit of claim 2, wherein said DSP controls a clock providing a timing signal at said preselected clock interval.

5. The circuit of claim 1, wherein said bank of shift registers comprises nine registers for storing nine incoming data.

6. The circuit of claim 1, wherein said coefficient registers comprises nine registers for storing nine coefficient values.

7. The circuit of claim 1, wherein said coefficient values are symmetric about a center coefficient.

8. The circuit of claim 1, wherein said coefficient values are asymmetric.

9. The circuit of claim 1, wherein said wavelet transformation circuit functions to provide up to a 9-stage finite impulse response (FIR) filter.

10. The circuit of claim 1, wherein said set of data inputs comprise high-pass inputs and low-pass inputs.

11. The circuit of claim 10, wherein said set of coefficient registers is loaded with coefficient values drawn from two different sets of coefficients, a high-pass set of coefficients employed for high-pass filtering and a low-pass set of coefficients employed for low-pass filtering.

12. The circuit of claim 11, wherein said high-pass set up coefficients and said low-pass set of coefficients are alternated, such that for a particular sequence of pixel values currently loaded in said bank of shift registers, only a single result is generated for either low-pass or high-pass.

13. The circuit of claim 1, wherein said set of coefficient registers stores a value of 0 in any coefficient register corresponding to an unused coefficient location.

14. The circuit of claim 1, wherein said bank of shift registers further comprises a multi-stage pipelined filter, such that each register position comprises a plurality of registers to be processed in parallel.

15. The circuit of claim 14, wherein said multi-stage pipelined filter comprises an 8-stage pipelined filter having eight parallel registers implemented at each register position.

16. The circuit of claim 15, further comprising a multiplexor circuit for controlling which particular parallel registers are multiplied against said set of coefficient registers at a given instance in time.

17. The circuit of claim 15, wherein said 8-stage pipelined filter is loaded in a burst of eight consecutive pixels in a horizontal line from the digital image, for application of a horizontal filter.

18. The circuit of claim 1, wherein said data inputs are shifted across said bank of shift registers, so that they can be multiplied against values stored by said set of coefficient registers.

19. The circuit of claim 1, further comprising:

a sub-sampling component for saturating down said result to a value having a preselected bit width.

20. The circuit of claim 20, wherein said result is saturated down to a16-bit value, by taking the most significant 16 bits of said result.

21. The circuit of claim 1, wherein said at least one result register comprises:

a low-pass result register for storing a low-pass result, and

a high-pass result register for storing a high-pass result.

22. The circuit of claim 21, further comprising a multiplexor circuit for controlling whether said result is placed in said low-pass result register or in said high-pass result register.

23. The circuit of claim 1, wherein said result comprises a new pixel value being determined from a then-current sequence of pixel values stored in said bank of shift registers and from said coefficient values stored by said coefficient registers.

24. The circuit of claim 1, wherein successive lines of pixel values are shifted in from the digital image, for application of a horizontal filter.

25. The circuit of claim 1, wherein successive columns of pixel values are shifted in from the digital image, for application of a vertical filter.

26. The circuit of claim 1, further comprising a mirroring function that mirrors data appearing at each end of a line of data being processed, during application of a horizontal filter.

27. The circuit of claim 1, further comprising a mirroring function that mirrors data appearing at each end of a column of data being processed, during application of a vertical filter.

28. The circuit of claim 1, wherein said circuit is implemented as an application-specific integrated circuit (ASIC).

29. The circuit of claim 1, wherein results obtained for the digital image are combined to produce a wavelet-based compressed image.

30. A method for performing high-pass and low-pass filtering required for a wavelet transformation, the method comprising:

storing a high-pass set of coefficient values for high-pass filtering, and a low-pass set of coefficient values for low-pass filtering;

shifting into a bank of shift registers a succession of pixel values from a digital image; and

as each successive pixel value is shifted in, alternating between

generating a high-pass result based on application of said high-pass coefficient values against the then-current pixel values stored by said bank of shift registers, and

generating a low-pass result based on application of said low-pass coefficient values against the then-current pixel values stored by said bank of shift registers.

31. The method of claim 30, wherein said steps operate under control of a digital signal processor (DSP).

32. The method of claim 31, wherein said pixel values are shifted in from a memory accessible to said DSP.

33. The method of claim 31, wherein said DSP controls a clock providing a timing signal at a preselected clock interval.

34. The method of claim 30, wherein said bank of shift registers comprises nine registers for storing nine incoming data.

35. The method of claim 30, wherein the two sets of coefficient values each comprise five coefficient values.

36. The method of claim 30, wherein each set of coefficient values is symmetric about a center coefficient.

37. The method of claim 30, wherein each set of coefficient values is asymmetric.

38. The method of claim 30, wherein said high-pass set up coefficients and said low-pass set of coefficients are alternated, such that for a particular sequence of pixel values currently loaded in said bank of shift registers, only a single result is generated for either low-pass or high-pass.

39. The method of claim 30, wherein said bank of shift registers operates in parallel with other registers to provide a multi-stage pipelined filter, such that each register position of said bank of shift registers comprises a plurality of registers to be processed in parallel.

40. The method of claim 39, wherein said multi-stage pipelined filter comprises an 8-stage pipelined filter having eight parallel registers implemented at each register position.

41. A wavelet filter circuit providing up to a nine stage finite input response filter, said circuit comprising:

a set of high-pass and a set of low-pass data inputs;

a bank of shift registers for storing data values received from said data inputs;

coefficient registers for alternately storing a set of coefficients for high-pass filtering and a set of coefficients for low-pass filtering; and

a multiplier/accumulator for applying coefficients stored in said coefficient registers against said data values in said shift registers to generate new values.

42. The circuit of claim 41, further comprising:

a sub-sampling component for saturating down said new values to result values having a preselected bit width.

43. The circuit of claim 41, further comprising:

a low-pass result register and a high-pass result register for storing said low-pass filtered and high-pass filtered result values, respectively.

44. The circuit of claim 41, wherein said wavelet filter circuit operates under the control of a digital signal processing (DSP) circuit.

45. The circuit of claim 44, wherein said DSP circuit controls a clock providing a clock tick at specified intervals.

46. The circuit of claim 41, wherein said data values input to said shift registers comprise pixel values from digital images.

47. The circuit of claim 46, wherein said shift registers comprises nine shift registers storing adjacent pixel values from a particular digital image.

48. The circuit of claim 41, wherein each register position of the register bank comprises a plurality of registers to be processed in parallel, for implementing a multi-stage pipelined filter.

49. The circuit of claim 48, wherein said multi-stage pipelined filter comprises an eight-stage pipelined filter having eight parallel registers at each register position.

50. The circuit of claim 49, wherein eight successive data values are written into said eight parallel registers at each said register position for parallel processing.

51. The circuit of claim 49, wherein use of high-pass and low-pass coefficients is alternated as each successive data value is read in for processing.

52. The circuit of claim 41, wherein said coefficients comprise pixel weightings.

53. The circuit of claim 41, wherein said set of coefficients include five high-pass coefficients and five low-pass coefficients.

54. The circuit of claim 41, wherein said wavelet filter circuit is configured to perform as a FBI 7-9 wavelet filter with zeros inserted in unused coefficient locations.

55. The circuit of claim 41, wherein input into said shift registers alternates input of successive data values from said set of high-pass data inputs and said set of low-pass data inputs.

56. The circuit of claim 55, wherein for a particular sequence of data values input into said shift registers, only a single result is generated for either high-pass or low-pass filtering.

57. The circuit of claim 41, wherein said coefficients stored in said coefficients register are symmetric around a center coefficient.

58. The circuit of claim 41, wherein only a single coefficient register a unique value.

59. The circuit of claim 41, wherein for a particular sequence of data values loaded in said shift registers, only a single result is generated for either high-pass or low-pass filtering.

60. The circuit of claim 41, further comprising a sub-sampling component that saturates down each new value to a 16-bit value.

61. The circuit of claim 60, wherein said sub-sampling component saturates down said new values to said 16-bit value by selecting the most significant 16 bits.

62. The circuit of claim 41, wherein said wavelet filter circuit renders wavelet-transformed versions of digital images.

63. A method for rendering wavelet-transformed versions of digital images, said method comprising:

inputting successive pixel values from a digital image into a bank of shift registers;

applying pixel weightings against the then current pixel values in said bank of shift registers, alternating between high-pass pixel weightings and low-pass pixel weightings to generate a set of high-pass values and a set of low-pass values, respectively; and

outputting said high-pass values and said low-pass values in a result register.

64. The method of claim 63, further comprising:

saturating down each said high-pass value and each said low-pass value to a result value to a pre-selected bit width.

65. The method of claim 64, wherein each said high-pass value and each said low-pass value is saturated down by selecting the most significant bits of said value.

66. The method of claim 65, wherein said shift registers comprise a bank of nine shift register positions, each said register position including eight parallel registers for parallel processing of pixel values.

67. The method of claim 63, wherein high-pass pixel weightings and low-pass pixel weightings are applied in an alternating fashion to the successive pixel values.

68. The method of claim 63, wherein said pixel weightings comprise a set of five high-pass weightings and a set of five low-pass weightings.

69. The method of claim 63, further comprising:

mirroring the pixel values at the start of each line of said digital image by copying the first four pixel values in reverse order after the fourth pixel value has been filled into said shift registers such that the filter receives symmetric data centered on the edge of the image.

70. The method of claim 63, further comprising:

mirroring the pixel values at the end of each line of said digital image by copying the last four pixel values in reverse order after the last pixel value has been filled into said shift registers such that the filter receives symmetric data centered on the edge of the image.